Please rewrite the description as follows: (A clean version of the applicable portion of the description is provided immediately below. Provided as an attachment to this amendment is a marked-up version of the prior pending applicable portion of the description with all changes shown.)

On page 1, between lines 3 and 4, please insert the following:

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a division of United States Patent Application Serial Number 09/517,292 filed 2 March 2000.

The paragraph starting on page 3, line 5:

Most of the development of bipolar junction transistors of silicon-on-sapphire has been concentrated in the area of lateral bipolar junction transistors, epitaxial vertical bipolar junction transistors, and heteroepitaxy bipolar junction transistors. This work has been recorded respectively by P.K. Vasudev in his article in the IEEE Circuits and Devices magazine titled: Recent Advances in Solid-Phase Epitaxial Recrystalization of SOS with Applications to CMOS and Bipolar Devices, of July 1987, pp. 17-19: by F.P. Heiman and P.H. Robinson in their article in *Solid State Electronics* titled: Silicon-on-Sapphire Epitaxial Bipolar Transistors of 1968, Volume 11, pp. 411-418; and by E.N. Cartagena, B.W. Offord and G. Garcia in their article in *Electronics Letters* titled: Bipolar Junction Transistors Fabricated in Silicon-on-Sapphire of 1992, Volume 28, pp. 983-985.

The paragraph starting on page 6, line 19:

Referring to FIGS. 1A and 1B, cross-sectional views of complimentary vertical bipolar junction transistors 10 fabricated of silicon-on-sapphire according to the invention are shown. The elements of these transistors will be discussed first. Following this will be a discussion of the steps used to fabricate these transistors.

The paragraph starting on page 9, line 15:

FIG. 9 illustrates a process used to create an N+ region in wafer 34 that is part of sub-collector region 26 of NPN vertical transistor 14 illustrated in FIG. 1. Photoresist layer 56 is produced by coating all of wafer 34 with photoresist and selectively removing the resist from certain regions of the wafer as is well-known to those knowledgeable in the art of semiconductor processing. Implantation to form the N+ region may utilize arsenic (As) ions for example at 80 KeV at a dose of $3x10^{15}$ ions/cm^2. Photoresist layer 56 prevents the ions from penetrating into region 58. However the As ions readily penetrate into region 60 of wafer 34.

In the Claims:

Please rewrite the claims as follows: (A clean version of the applicable portion of the claims is provided immediately below. Provided as an attachment to this amendment is a marked-up version of the prior pending applicable portion of the claims with all changes shown.)

Please cancel claims:12-18.